REMARKS

Claims 1-20 were pending in the application prior to the present amendment.

Claims 3, 7-8, 14-15 and 17-19 are herein cancelled.

Claims 1, 12-13 and 16 are herein amended.

Claims 26-28 are added.

Thus, claims 1-2, 4-6, 9-13, 16 and 20-28 will be pending after entry of the present amendment.

Claims 3, 7, 8, 18 and 19 were indicated to be allowable if rewritten in independent from including all the limitations of their respective based claims and any intervening claims. Thus, independent claims 1 and 16 have been amended as follows:

claim 1 has been amended to include the material of former claim 3;

claim 16 has been amended to include the material of former claims 17 and 18.

New independent claim 26 incorporates the language of claim 1 and former claim 7.

New independent claim 27 incorporates the language of claim 1 and former claim 8.

Therefore, claims 1, 16, 26 and 27, and their dependents, are now in condition for allowance.

Independent claims 12 and 13 have each been amended to add the material of former claim 3. (Claim 3 was indicated to be an allowable dependent of independent claim 1.)

New independent claim 28 incorporates the language of independent claim 16 and allowable dependent claim 19, but does not incorporate the language of intervening claim 17.

Art Rejections

Claims 1, 2, 4-6, 9, 11-17 and 20 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Sunter (USPN 6,492,798).

Claim 10 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Sunter (USPN 6,492,798).

Applicant respectfully traverses these rejections based on the following reasoning.

Claim 12 as amended herein recites:

> "An integrated circuit including logic for testing internal operation of the integrated circuit, the integrated circuit comprising:
>
> a plurality of internal functional blocks coupled by a plurality of internal buses, wherein the plurality of internal functional blocks and the plurality of internal buses are comprised in the integrated circuit;
>
> at least one test control input pin comprised on the integrated circuit;
>
> a set of test output pins comprised on the integrated circuit; and
>
> selection logic comprised in the integrated circuit, wherein the selection logic comprises: a plurality of inputs coupled to two or more of the plurality of internal buses; at least one select input coupled to receive at least one select signal from the at least one test control input pin; and an output coupled to the set of test output pins; wherein the selection logic is operable to select internal bus signals from one of the two or more internal buses based on the at least one select signal from the at least one test control input pin, wherein the selection logic is configured to output the selected internal bus signals to the set of test output pins;
>
> interface logic coupled between at least one of the plurality of inputs of the selection logic and at least one of the plurality of internal buses, wherein the interface logic is configured to buffer data from the at least one internal bus before the data is output to the set of test output pins."

This combination of features is not taught or suggested in Sunter. In particular, Sunter never teaches or suggests "interface logic coupled between at least one of the plurality of inputs of the selection logic and at least one of the plurality of internal buses, wherein the interface logic is configured to buffer data from the at least one internal bus before the data is output to the set of test output pins." Thus, claim 12 is patentably distinguished over Sunter.

Claim 13 as amended herein recites:

> "An integrated circuit including logic for testing internal operation of the integrated circuit, the integrated circuit comprising:
>
> a plurality of internal functional blocks coupled by a plurality of internal buses, wherein the plurality of internal functional blocks and the plurality of internal buses are comprised in the integrated circuit;
>
> at least one test control input pin comprised on the integrated circuit;

a set of test output pins comprised on the integrated circuit; and

selection logic comprised in the integrated circuit, wherein the selection logic comprises: a plurality of inputs coupled to two or more of the plurality of internal functional blocks; at least one select input coupled to receive at least one select signal from the at least one test control input pin; and an output coupled to the set of test output pins; wherein the selection logic is operable to select internal functional block signals from one of the two or more internal functional blocks based on the at least one select signal from the at least one test control input pin, wherein the selection logic is configured to output the selected internal functional block signals to the set of test output pins;

interface logic coupled between at least one of the plurality of inputs of the selection logic and at least one of the plurality of internal buses, wherein the interface logic is configured to buffer data from the at least one internal bus before the data is output to the set of test output pins."

This combination of features is not taught or suggested in Sunter. In particular, Sunter never teaches or suggests "interface logic coupled between at least one of the plurality of inputs of the selection logic and at least one of the plurality of internal buses, wherein the interface logic is configured to buffer data from the at least one internal bus before the data is output to the set of test output pins." Thus, claim 13 is patentably distinguished over Sunter.

New claim 28 recites:

"An application specific integrated circuit, comprising:

a plurality of functional units;

a plurality of internal buses connecting the functional units;

one or more control pins;

a plurality of test pins; and

multiplexing logic coupled to at least a subset of the plurality of internal buses and the test pins, wherein the multiplexing logic is configured to select one of the plurality of internal buses in response to one or more control signals conveyed to the multiplexing logic from the control pins, wherein the multiplexing logic is configured to output signals from the selected internal bus to the test pins in real-time;

wherein the test pins are configurable for non-test use by a control signal delivered to the selection logic via the one or more control pins."

This combination of features is not taught or suggested in Sunter. In particular, Sunter never teaches or suggests "the test pins are configurable for non-test use by a control

signal delivered to the selection logic via the one or more control pins." Thus, new claim 28 is patentably distinguished over Sunter.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5181-90200/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Request for Approval of Drawing Changes

☒ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,

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Date: 2/12/2004